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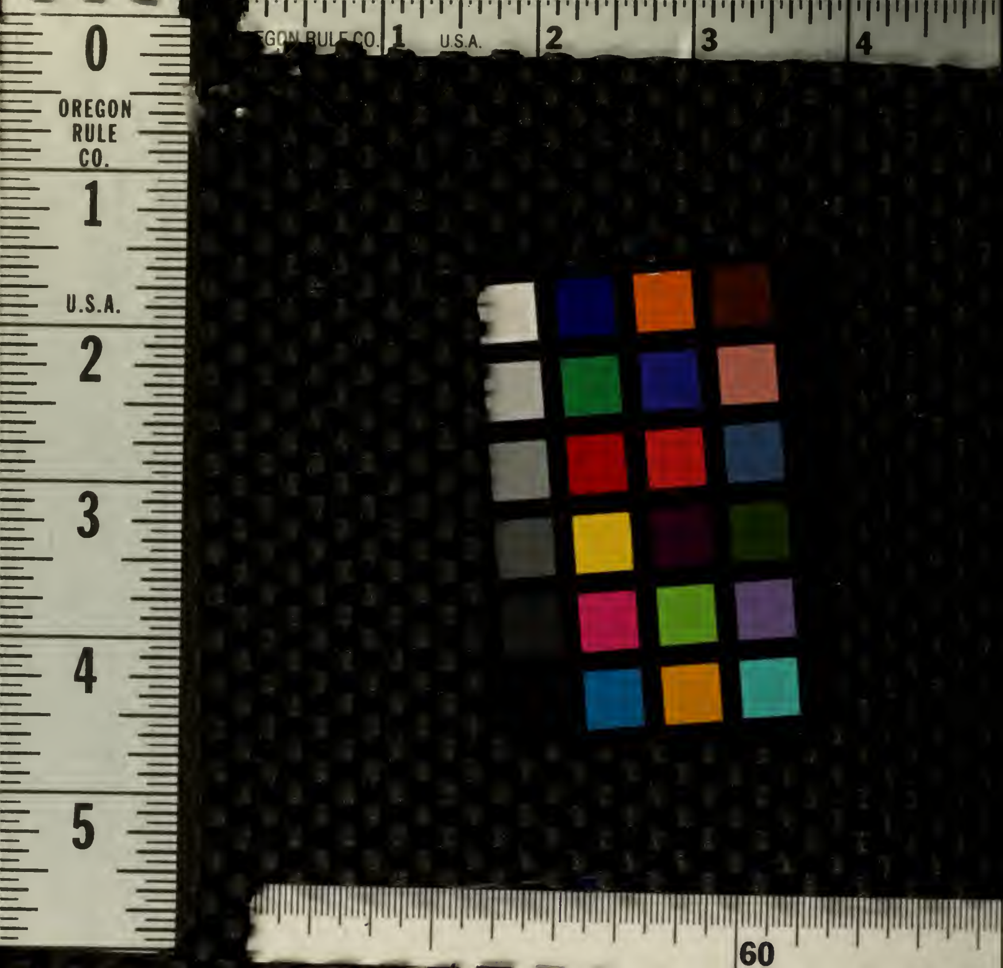

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METHOD FOR CONVERSION OF ANALOGUE DATA TO DIGITAL DATA

BY

LESLIE H. SELL

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A METHOD FOR CONVERSION OF ANALOGUE DATA TO DIGITAL DATA

by

Leslie N. Sell
Lieutenant, U. S. Navy

Submitted to the faculty of the Moore School of Electrical Engineering as a part fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

Philadelphia, Pa.
1949

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FOREWORD

Part I of the thesis contains a discussion of the generalized problem and the techniques and components available for the design of an analogue to digital data converter.

Part II consists of the explanation of the schematic diagrams and circuit operation of the converter and its associated equipment.

Part III concludes the thesis with the presentation of test data and the conclusions resulting thereby.

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I. PRELIMINARY DISCUSSION

1.1 Introduction.

In many applications, both civilian and military, the need arises for a system of information transmission of extreme rapidity and accuracy. The most widely used system possessing these characteristics is the closed loop synchro transmission system. However this method requires physical connections between the component units with the consequent prohibition of both long separation distances and relative translation of the component units.

To remove these restrictions the following paper outlines a method of binary encoding of analogue data, obtainable from the rotational position of an output shaft of the unit providing the information to be transmitted. The resulting binary number is held in a static memory storage unit from which, by the use of high speed digital calculating techniques, it could be used for frequency shift keying of a transmitter. Suitable techniques are likewise available for the decoding of the signal at a receiving station, and the consequent visual presentation of the desired information on either a binary or decimal basis. Moreover, since the encoding and storage is continuously repeated at a 60 cycle rate the transmitted information, although quantized, appears continuous for information variation frequencies considerable lower than 60 cycles, as will be the usual case.

1.2 Generalized System Discussion.

(a) Overall System - The basic process of binary encoding is outlined in figure 1. A trigger pulse is introduced simultaneously into three units to (a) start the sweep of a movable time marker generator, (b) operate the clearing section of a binary counter and thereby reset the total count to zero, and (c) set a flip-flop circuit which opens a gate interposed between a fixed frequency oscillator and a binary counter, thus causing the counter total to increase linearly with time. After a time interval determined by the rotational data input (analogue data) the movable time marker generator emits a pulse, resetting the flip-flop and closing the gate to the counter. The total count reached by the binary counter will thus be a joint function of the frequency of the oscillator and the time interval between the trigger pulse and the movable time pulse.

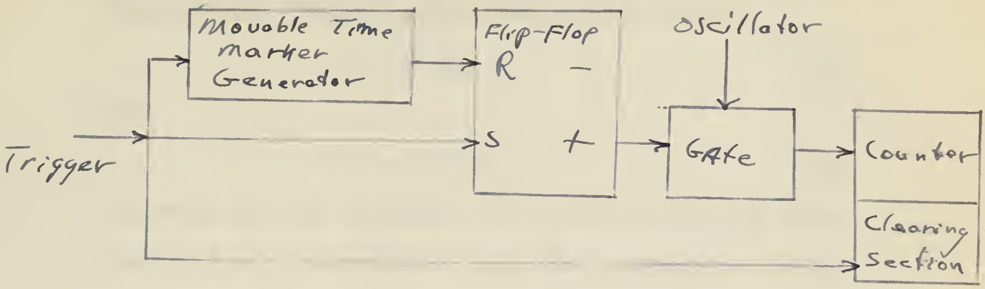

Fig. 1. Block diagram of analogue data converter.

$$D_b = ft \qquad (1)$$

where D_b is the information encoded on a binary basis

and t is the time duration between trigger and marker pulse expressed in units of the oscillator period T. If the operation of the movable time marker circuit is linear with respect to analogue data input

$$t = k\ D_a \qquad (2)$$

and

$$D_d = \int k\ D_a \qquad (3)$$

where D_a is the analogue data input and k is the constant of proportionality. The subsequent introduction of a second trigger pulse will cause a repetition of the entire cycle, resulting in the same total count for an unchanged input or a different count for a changed input. Thus triggering on a cyclic basis is feasible and, as will be developed later, highly desirable.

(b) Introduction of analogue data - In the vast majority of cases, the information to be encoded can be obtained as mechanical motion of a data measuring or recording device. It may occur as the motion of the range knob of a range measuring device, the motion of the input crank to a zero reader dial, the control knob used in balancing an electrical bridge used as a measuring device, the linear movement of an index against a scale, or in numerous other manners. In all these cases however, it is apparent that the motion of the measuring device can be used to control the position of the movable arm of a potentiometer. Thus the analogue positional data can be converted into a voltage signal suitable for introduction into the movable time marker generator.

(c) Movable time markers - In general, four methods of obtaining continuously movable time markers are commonly used. In increasing order of precision obtainable with respect to time, they are:

(1) the cathode-coupled multivibrator,

(2) the phantastron,

(3) a timing circuit based on a linear sawtooth,

(4) the phase-shifting of a precision sinusoid.

Quite naturally, increase in precision is obtainable only by increase in complexity of the circuitry involved.

Since it is desired to achieve an overall system performance comparable in accuracy to that of a synchro system (roughly 2 parts in 360), a movable time marker system permitting this degree of accuracy must be selected. Methods (2), (3), and (4) all meet this requirement but method (4) involves too much complexity for the result desired. Thus either method (2) or (3) appears suitable. From general considerations the latter was chosen for use in the data converter system covered by this paper.*

Through the use of the selected sweep circuit time may be represented by the voltage rise of a linear

---

* Parallel development of a system using the phantastron circuit is covered by a Master's thesis "Conversion of Range or Bearing into Binary Data by Use of a Cyclic System" by L. Grabowsky and W. L. Benbow.

sawtooth wave above a zero reference level. Continuous comparison of the magnitude of the sawtooth against the signal voltage corresponding to the analogue data permits the generation of a marker pulse whenever equality exists. Thus a signal pulse may be generated which is delayed from zero reference time by an interval proportional to the signal voltage level of the input data.

(d) Comparator - A comparator is a device capable of performing amplitude selection. Of the several types in common usage the diode selector shown in figure 2 is almost universally used for the selection and reproduction of a portion of a waveform where accurate evaluation of boundary setting is of importance. The DIODE selects the portion of the sawtooth waveform above the reference voltage thereby causing an attenuated reproduction of the selected portion of the sawtooth to appear at the diode cathode. This positive signal is quasi-differentiated in the grid circuit of the following tube, amplified, and further differentiated in the amplifier output. Further stages

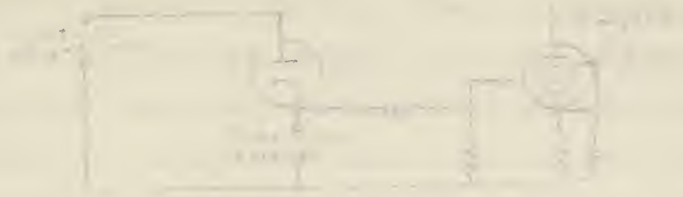

Fig. 2. Single diode comparator

of amplification and pulse shaping may be necessary to ultimately produce a pulse marker corresponding in time to the moment of conduction of the diode.

Although the aforementioned single diode comparator was selected as being most suitable for use in the data converter serious consideration was given to the double diode comparator shown in figure 3.

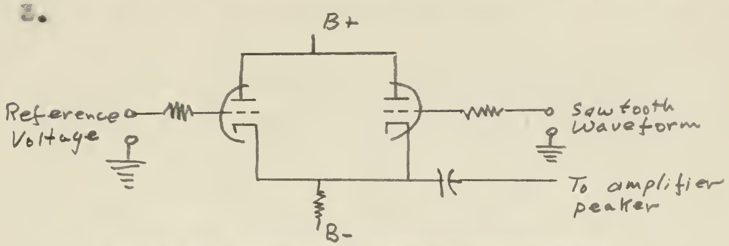

Fig. 3. Double triode comparator

Even though the break instability for a grid tube is greater than for a diode and hence the boundary setting is not as accurately defined, this type of comparator will give amplitude selection to within 1/10 volt. Since the sawtooth rise time of the designed system is in excess of .025 volts per micro-seconds and the oscillator frequency is 100kc the sawtooth rise between successive cycles of the oscillator is 2½ times the break instability. Thus this type of comparator should give as great accuracy as the diode and may be more desirable from amplification considerations.

The use of crystal rectifiers was considered since they possess slightly greater break stability than thermionic diodes. Since the back current was undesirable and the increase in sensitivity was not necessary the crystals were not used.

(c) Counters - The scale of two binary counters occur in many varying forms, but all are essentially modified Eccles-Jordon circuits. The two basic methods of triggering, grid and plate, determine the specific circuit design. A simple grid triggered circuit developed by Potter* is shown in figure 4. The upper

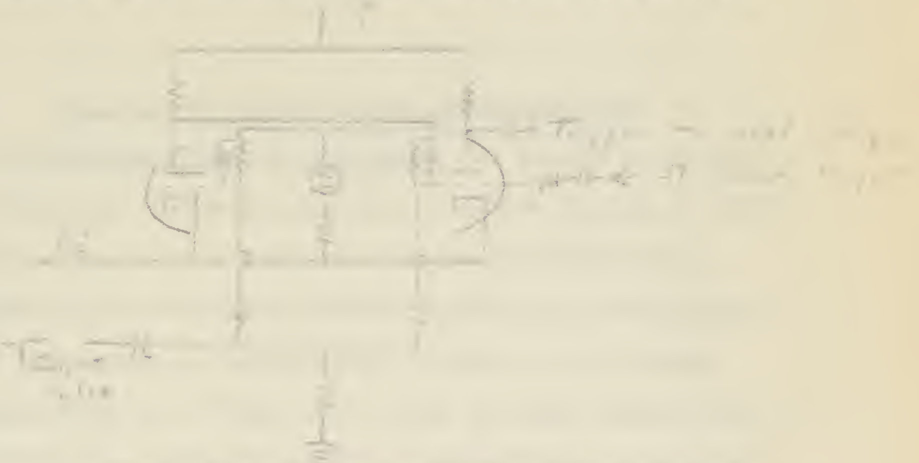

Fig. 4. Grid triggered binary counter stage

limit of multiple stage operation is 10kc and the triggering and resetting difficulties at this rate of counting make the circuit unfeasible. For lower rates of operation, however, this circuit should prove feasible. The plate triggered counter shown in figure 5 achieves reliable operation at 10kc, and is the circuit selected for the converter. Increase in reliability of operation and frequency limit attainable may be obtained through the use of buffer coupling stages.

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* See bibliography

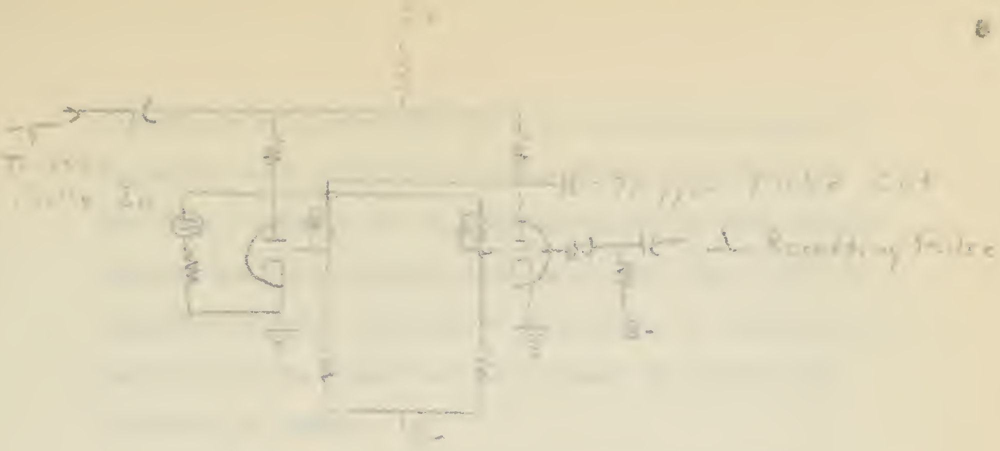

Fig. 5. Plate triggered binary counter

(f) Cyclic rates of operation - In the overall information transmission and reception system of which the analogue data converter comprises the initial major unit, the most probable method of presentation of the received information will be a visual one, consisting of a "read out" array of neon indicators, operated in either binary or decimal code as may be desired. If the data converter be triggered with a period less than the retentivity period of the human eye, the visual presentation will appear to represent continuous rather than intermittent information. Moreover, the effects of momentary errors in encoding and imperfect reception will be minimized. These considerations led to the adoption of a trigger frequency of 60 cycles, giving an inter-trigger interval of 16,666 micro-seconds.

In conjunction with the above two considerations developed in earlier sections should be remembered. It was decided that satisfactory counter operation could be obtained as high as 100kc and that the

maximum count necessary to cover the full range of analogue data should be of the order of 360. Thus the time required for a maximum count is 3600 micro-seconds and the maximum duty cycle is 1/3. This is satisfactory for the proper operation of the linear sweep circuit. Hence the oscillator frequency may be fixed at 100kc.

It must be noted that the counter becomes a static memory storage tank for the total count during the interval between completion of counting and retriggering of the entire system. It is during this interval that the counter should be used to control a matrix array of time sequenced gates and thereby modulate the r.f. carrier. Since digital computing machines are currently in operation at megacycle rates the associated techniques would permit the completion of modulation and transmission of the encoded information (consisting of nine binary digit positions) in 10 micro-seconds or less. Hence the required transmission time is independent of the time required to encode the data and therefore the encoding may be done at the comparatively slow 100kc rate. Since the duty cycle for the transmitter is 10/10,800 it is apparent that a great deal of multiplexing can be accomplished.

(g) Increasing data accuracy - The limit of the accuracy in the data transmitted will depend primarily upon the precision with which the original data can

be measured. The magnitude of the incremental change in analogue data corresponding to a unit change in the digital data can be increased or decreased by a corresponding change in the comparator circuit, affecting either oscillator frequency or sawtooth slope. A great improvement in accuracy may be obtained from the use of a multi-speed system similar to that used in synchro transmission systems.

II. EXPERIMENTAL APPARATUS

2.1 Explanation of circuits used.

(a) *Block diagram* - In PLATE I is shown a block diagram of the experimental apparatus used. To obtain sufficient data both cyclic and one shot operation is required. A 60 cycle square wave generator (H. P. Model 210-A) provides a suitable cyclic triggering waveform, and a controlled flip-flop provides a single signal when desired. The triggering waveform is shaped by the amplifier into a sharply rising spike which sets the flip-flop and simultaneously zeros the counter. The setting of the flip-flop opens the tube gate, allowing 100kc pulses to start the counter operating. The triggering waveform is applied also to the sawtooth generating circuit to produce a linear voltage sweep output. This is compared with the voltage level generated by the helipot which introduces analogue data and a suitably delayed pulse is emitted from the comparator. This pulse closes the tube gate and stops operation of the counter, allowing the total count to remain static and readable on the neon indicators.

(b) *Linear sweep and comparator circuit* - PLATE II is the schematic of this circuit, while figure 6 sketches the critical waveforms. The triggering square wave (1) (a positive pulse of at least 5 volts amplitude would be equally acceptable as a trigger) is amplified in V1, which is biased beyond plate current cutoff.

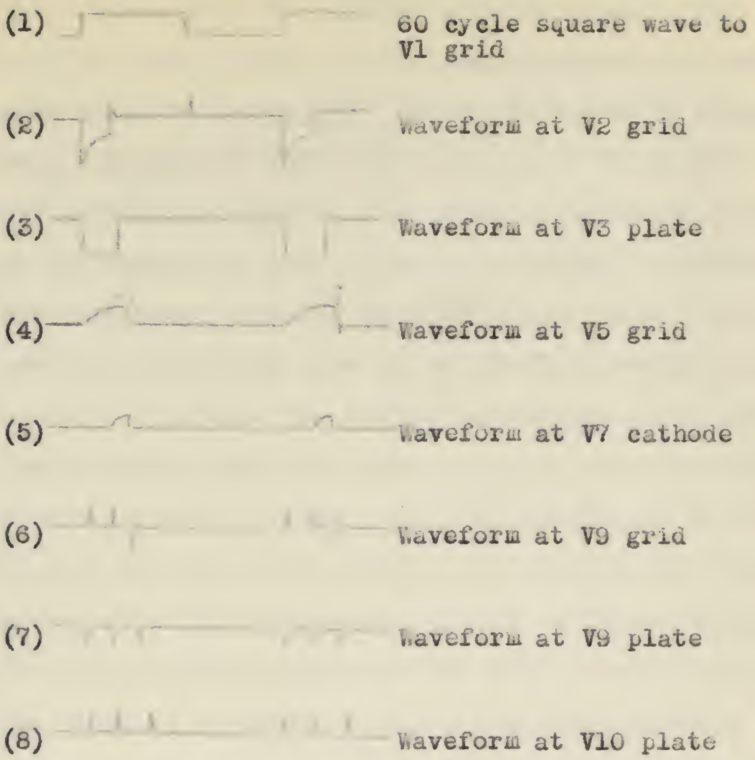

Fig. 6. Critical waveforms in the linear sweep and comparator circuit

Since a pentode is used, the trigger causes the tube to conduct strongly and a large negative pulse appears at the plate. This negative pulse is applied to a monostable multivibrator V2,V3 which generates the 4000 micro-second negative gate pulse shown in (3) above. This type of circuit is used because it is less susceptible to changes of gate duration and amplitude caused by tube changes than are cathode coupled circuits. The negative gate at the plate of V3 is direct coupled to the grid of V4, which acts

as a switch tube. The direct coupling enables the start of the switch action to be independent of the repetition frequency. The triode switch V4 is closed except during the 4000 micro-seconds which follow the initiating trigger. The sawtooth generator responds to the opening of the switch by producing a voltage that increases linearly with time. The circuit is a bootstrap generator plus an integration network, which tends to eliminate the second derivitive of the saw-tooth voltage rise and hence increases the linearity of the waveform. A linear rise (4) occurs at the grid of tube V5 and a rise which is less linear but which occurs at a lower impedance appears at the cathode. The grid waveform serves as the input to the comparator. The diode V7 selects the rise above the reference voltage level from the helipot and the distorted and clipped peak of the sawtooth appears at the cathode of V7 (5) . Quasi-differentiation in the grid circuit of the amplifier V8 and further differentiation in the input to V9 produces the ultimate waveform (6) at the plate of V9. Of the three pulses which comprise the output group only the center one is of consequence. The left pulse of the group occurs at the reference time (when trigger is introduced into the system) and is due to imperfect voltage regulation of the system. The effect of this pulse on the flip-flop controlling the gate tube is overridden by the SET pulse which simultaneously enters that circuit. The center pulse

is the one which is movable in time phase and may be moved over the entire range between the first and third pulses. This pulse RESETS the gate flip-flop. The third pulse is due to differentiation of the voltage overshoot in the amplifier V8 occurring when the sawtooth abruptly falls to its initial value. However, since the flip-flop has already been RESET by the movable marker, this pulse produces no effect.

The circuit accuracy depends primarily upon the capacitors C7 and C8, the helipot R17, the resistor R14, and the various vacuum tube switches. The sawtooth nonlinearity is less than .1% and the helipot is accurate to within .1%. Thus the attaining of the desired system accuracy (0.5% or better) becomes dependent primarily upon the amplitude selection ability of the diode V7 and the following amplifiers.

(c) Binary counter circuit - The circuit used for the construction of an individual stage of the binary counter is shown in PLATE III. Nine such stages are connected in tandem to permit a total count of 511. Introduction into V3 of a positive pulse from the tube gate circuit (or the preceding stage for the subsequent stages) causes V3 to conduct momentarily, lowering the potential applied to the plate resistors of V1 and V2. Through the usual mechanism of flip-flop action this causes the conducting tube to become non-conducting and vise-versa. Introduction of a

second pulse into V3 will again flip V1 and V2, restoring original conditions. Whenever V2 becomes conducting a positive pulse triggers V4, thus operating the second stage of the counter. It is apparent that each stage will operate at one half the frequency of the preceding stage, and the inclusion of neon indicators as shown permits the circuit to be used as a binary counter.

Since provision must be made for returning the counter to zero at the beginning of each count, thereby requiring that tube V2 of each stage be cut-off, the SST trigger pulse is applied to C6. The cathode connection of the 1N34 crystal is connected to the grid of V1 and the crystal plate is biased well below the normal voltage excursion of the grid of V1. Introduction of the SST pulse raises the crystal plate above ground potential, thereby causing V1 to conduct and V2 to be cut off. As V2 is cut off it creates an output pulse tending to trigger the following stage, but this effect is overridden by the signal being applied to the V1 grid of that stage.

In the latter stages of the counter the operating frequency is greatly reduced and the allowable time constants are much longer. This permits the use of larger values of grid and interstage coupling capacitors if an improvement in reliability of performance is considered necessary.

(d) Flip-flop and tube gate circuit - This circuit, which controls the input to the counter, is shown in PLATE IV. V1 and V2 comprise a flip-flop controlled by tube V3. Introduction of the positive SET pulse into C3 will cut off V1 and cut on V2 while a positive RESET pulse into C2 will cut off V2 and cut on V1. The circuit constants of the flip-flop are so chosen that the plate of V1 swings between minus 15 and plus 25 volts and this potential is resistance coupled to the second control grid of tube V4. As the cathode of V4 is at plus 10 volts, the action of the flip-flop swings the second control grid to a potential which is either below cutoff or above cathode potential. The output from the 100kc oscillator (a Measurements Corporation Pulse Generator Model 79-B was used in the experimental set-up) is fed into the first control grid of V4, so that output negative pulses are obtained at the plate whenever the flip-flop swings the second control grid positive. These pulses are inverted in amplifier V5 to provide the positive pulses suitable for driving the counter.

The cyclic operation of the gate consists of (1) the introduction of the SET pulse generated from the 60 cycle trigger, with consequent opening of gate V4 and introduction of pulses to the counter, and (2) the arrival of the output pulse from the comparator to reset the flip-flop and shut the gate.

(e) Miscellaneous circuits - PLATE V shows the two remaining components of the overall system - the SET pulse amplifier and wave shaper and the pulse source for one shot operation.

Tubes V1 and V2 comprise a two stage amplifier capable of producing a sharply rising positive pulse of sufficient amplitude to drive the large load on the SET pulse. The output from a square wave generator is used to drive the amplifier but operation would be equally satisfactory for triggering by a sharp spike.

Tubes V3 and V4 comprise a flip-flop. Closing of switch S1 causes V3 to conduct and V4 to be cut off. The resultant rise in plate voltage of V4 produces a suitable signal for one-shot operation of the entire system. Less complicated switching circuits would produce the same result but the use of the multivibrator circuit produces faster switching times and hence sharper rising output waveforms.

III. RESULTS AND CONCLUSIONS

3.1. One shot operation.

To permit evaluation of the system linearity, test data was obtained for non-cyclic operation, through the use of the single trigger pulse source. The variable resistors R16 and R18 of the comparator circuit, which control the maximum and minimum counts obtainable, were adjusted until the analogue data range 0 to 300 corresponded to a 7 to 306 range output on the counter. The digital data scale could have been adjusted to a 0 count for minimum analogue data setting but this was not done in order to obtain definite counts at the minimum position. The data obtained is listed on TABLE VI and is graphed on PLATE VII. The error in linearity is too small to detect in the data taken and is certainly within the desired 0.5%. It should be noticed that for each setting of the helipot there are two numbers differing by only one count. This is due to the oscillator not being synchronized with the trigger pulses. Thus the first pulse to be counted may occur anytime within the first 10 micro-seconds after the triggering pulse. Since the flip-flops and gate require an appreciable amount of time for operation (a few micro-seconds), a pulse which occurs too quickly following the trigger pulse will not get through the gate. Thus the count will vary between two numbers. Synchronizing the pulser and oscillator will remove

this variation, but such a procedure is not necessary to obtain the desired accuracy. In the listed data there may be noted an occasional error of 2 counts. This is believed due to the counter, the proper operation of which occasioned more difficulty than any other piece of equipment. Earlier runs, for which data is not shown, produced the same general results as the included data but contained numerous errors, usually all multiples of a single number such as 4. This indicated intermittent operation of some stage of the counter. Repeated adjustments of the counter eliminated these repeating errors, and all available tests indicated satisfactory performance by the counter during the single pulse data run.

3.2 Cyclic Operation.

The operation of the converter system on a cyclic basis cannot be termed fully successful, and no data of an experimental nature is presented. When the output of the tube gate was viewed on a CRO the cyclic operation of the comparator system appeared completely satisfactory. A uniformly varying gate was obtained for corresponding variations in helipot setting and, in so far as the pulse count could be made on a CRO, appeared to yield results in complete conformity with that obtained under one shot operation. Similar operation could not be obtained with the counter. The performance of the counter

resetting system was not satisfactory and the operation was too intermittent to permit taking consistent data over the entire helipot range. For counts totaling 64 and under, observable results were obtained by disconnecting the last three stages of the counter. The output appeared linear and in conformity with single pulsed operation except that the cyclic total count for each setting of the helipot was from 1 to 3 counts below that obtained by the single pulse operation. This is believed due to the time constants in the zeroing circuit being larger than the counting pulse interval, causing one or more counting pulses to be overridden by the zeroing pulse. All attempts to decrease the time constant of the zeroing circuit resulted in less satisfactory operation of the counter.

3.3 Conclusions.

The results obtained indicate that the basic premise is correct and that conversion of analogue to digital data is feasible. For a transmission system where single pulsed operation only is required, the relatively simple system designed herein is adequate. For the more realistic cyclic transmission system a definite need is indicated for the two following steps:

(a) Improvement of the zeroing circuit of the binary counter is essential.

(b) Improvement of the amplification stages of the comparator, such as the use of pulse transformers for coupling, should increase amplitude selection.

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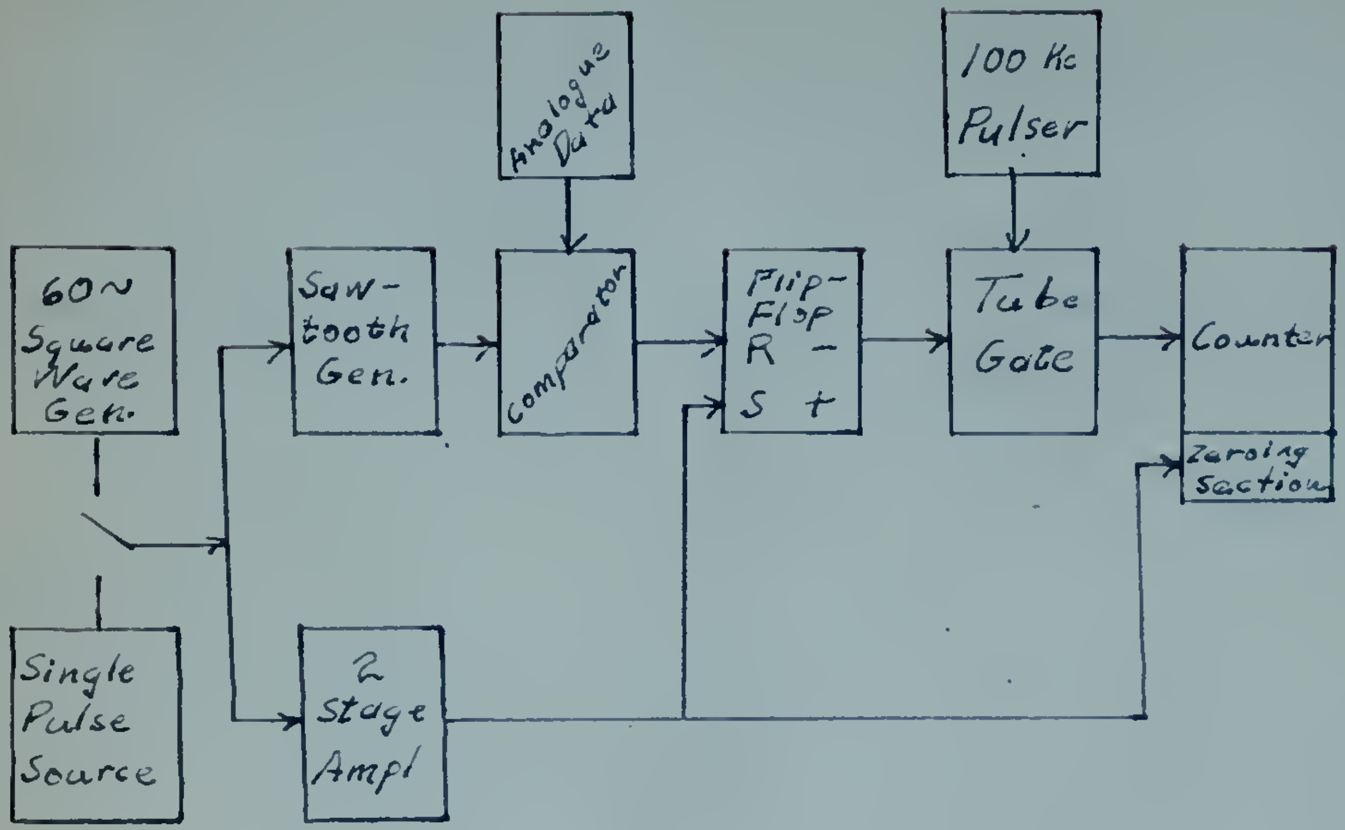
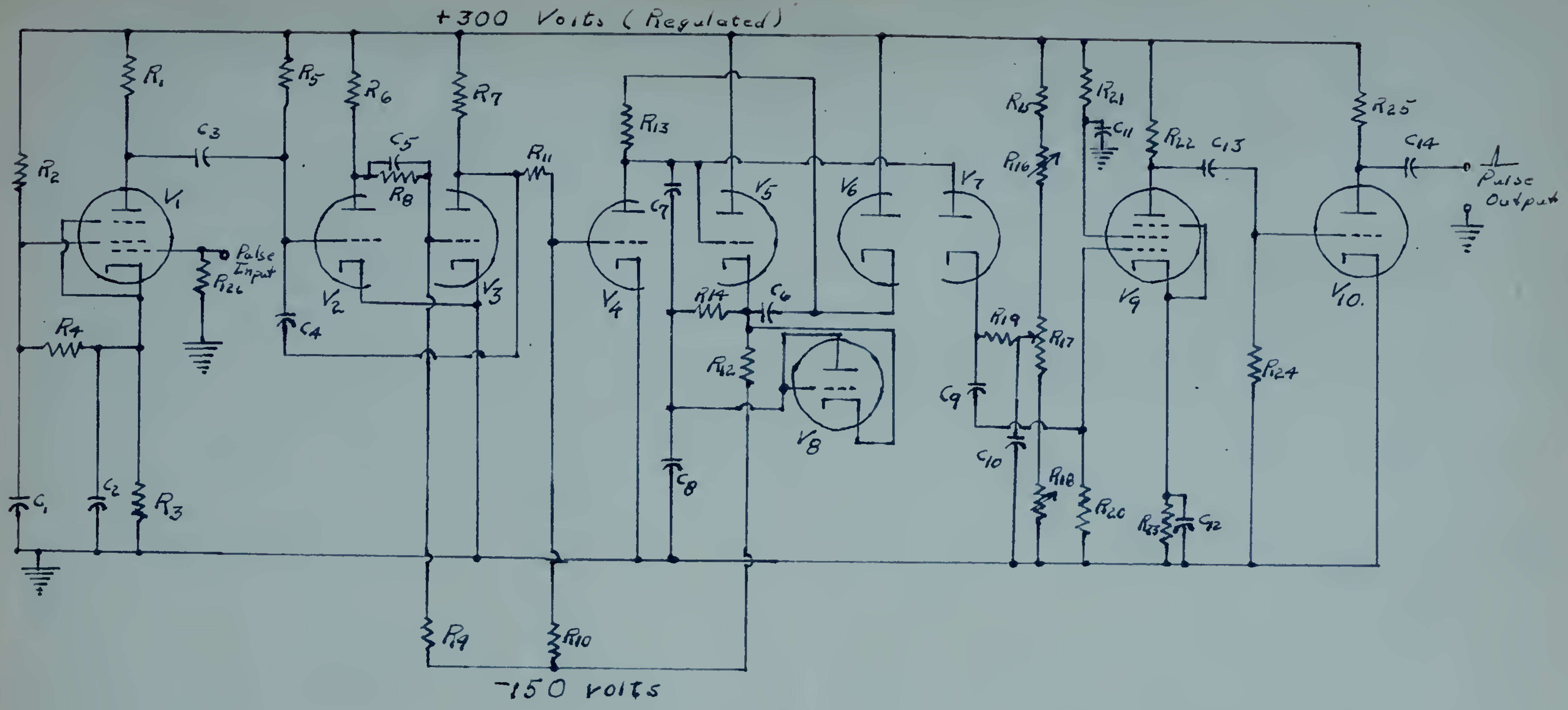


PLATE I

Block diagram of Data Converter

PLATE I

Block diagram of Data Converter



R1 -100K
R2 -150K
R3 -4.7K
R4 -150K
R5 -1M
R6 -50K
R7 -22K
R8 -300K
R9 -300K
R10-100K
R11-150K
R12-22K
R13-250K

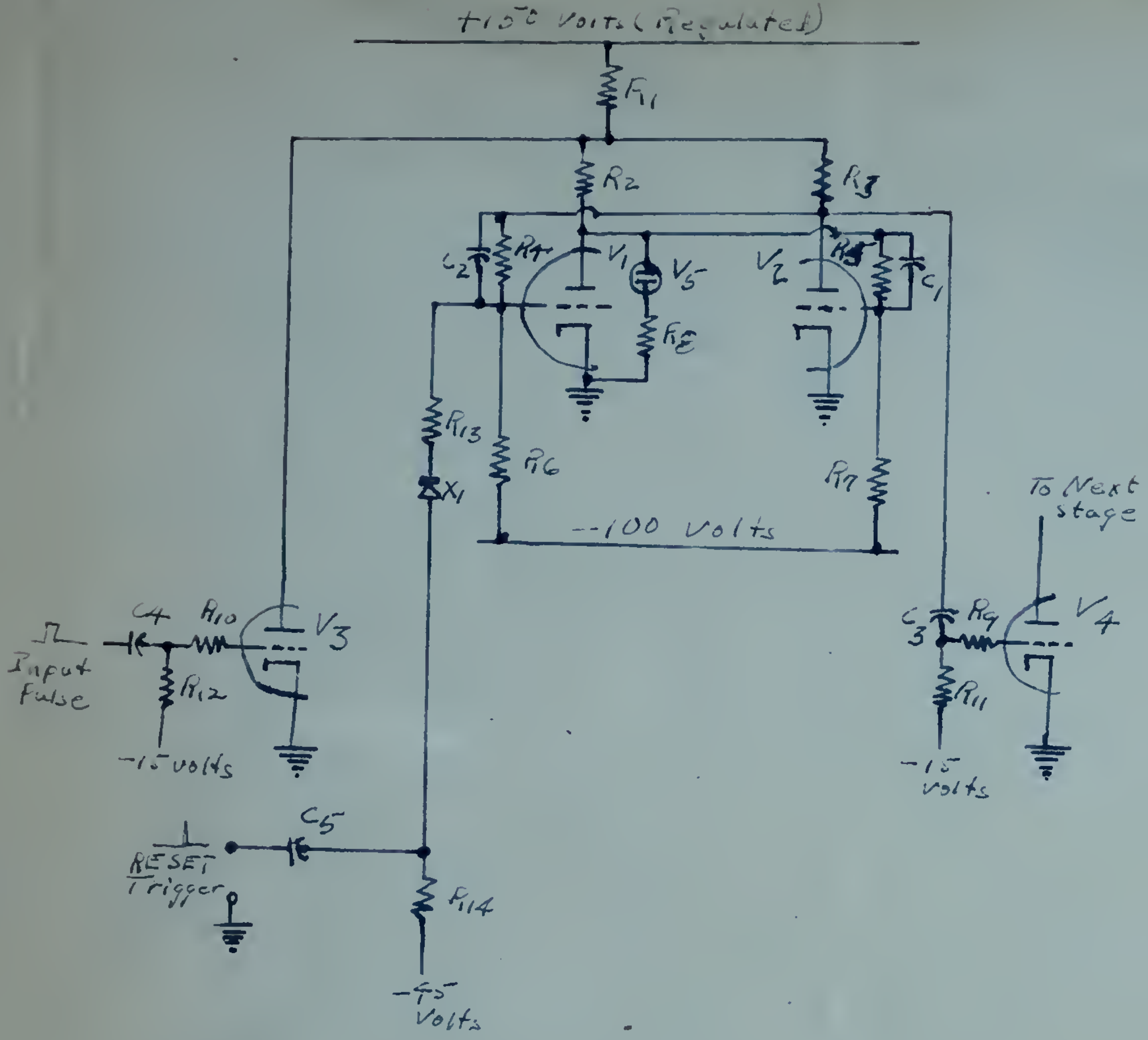
R14-350K
R15-22K
R16-10K Pot
R17-30K Helipot
R18-5K Pot
R19-10K
R20-22K
R21-100K
R22-22K
R23-56
R24-47K
R25-270K
R26-.1M

C1 -.01μf
C2 -.01μf
C3 -50μμf
C4 -.007μf
C5 -50μμf
C6 -.4μf
C7 -.08μf
C8 -.08μf
C9 -360μμf
C10-.001μf
C11-.01μf
C12-.1μf
C13-.004μf
C14-50μμf

V1 -6AC7
V2 -½6SN7
V3 -½6SN7
V4 -½6SN7
V5 -½6SN7
V6 -½6H6
V7 -½6H6
V8 -½6SN7
V9 -6AC7
V10-½6SN7

PLATE LL

Linear Sweep and Comparator Circuit



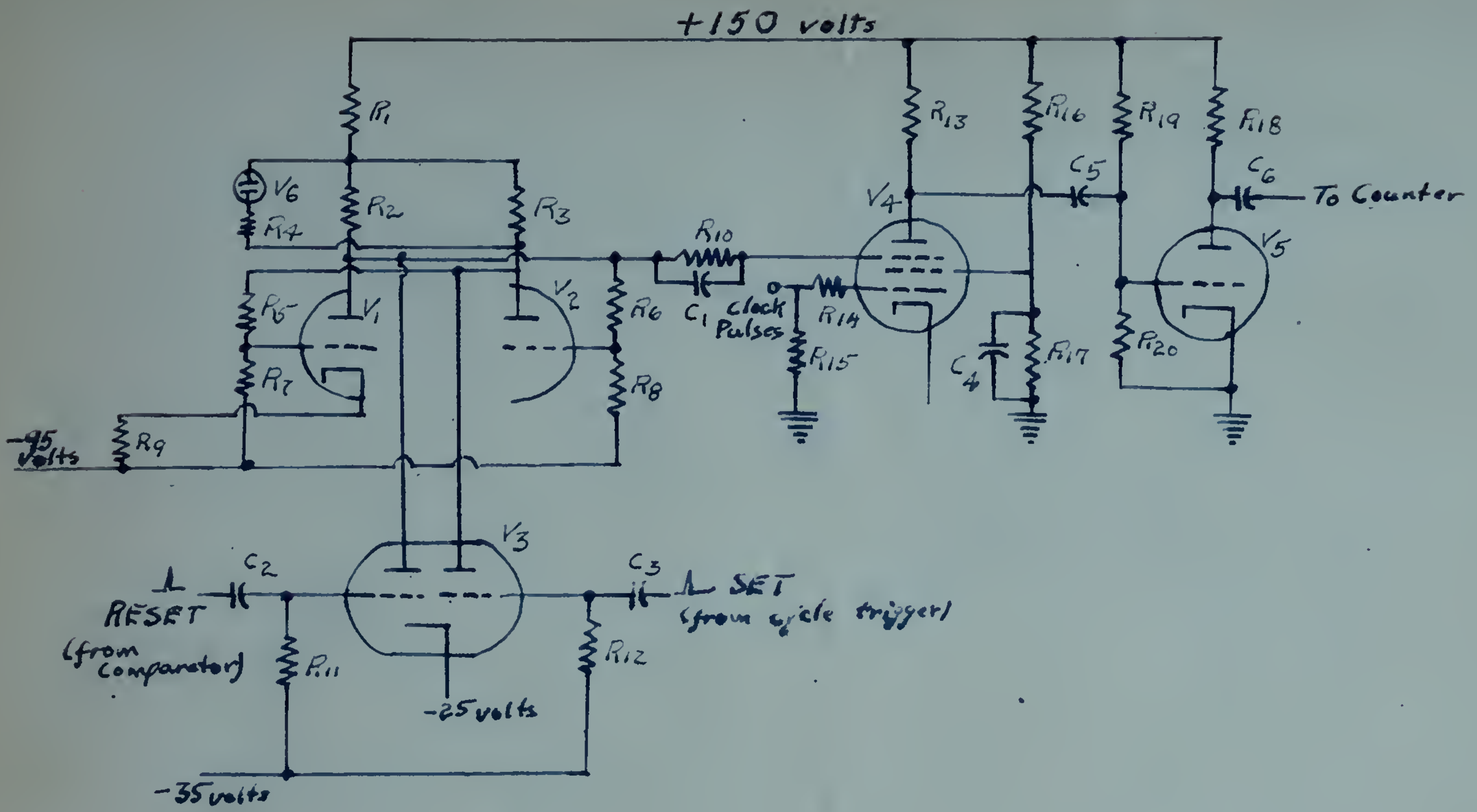
R1 - 8.2K
R2 - 8.2K
R3 - 8.2K
R4 - 47K
R5 - 47K
R6 - 82K
R7 - 82K
R8 - 82K

R9 - 4.7K
R10- 4.7K
R11- 47K
R12- 47K
R13- 4.7K
R14- 500K Pot
C1 - 50μμf
C2 - 50μμf

C3 -50μμf
C4 -50μμf
C5 -.008μf
X1 -1N34 Crystal
V1,V2,V3,V4
-$\frac{1}{2}$6SN7
V5 -Neon Bulb

PLATE III

Binary Counter Stage



R1 -15K
R2 -27K
R3 -27K
R4 -270K
R5 -27K
R6 -27K
R7 -100K
R8 -100K
R9 -18.2K
R10-100K
R11-47K
R12-47K
R13-4.7K
R14-4.7K
R15-47K

R16-41K
R17-185K
R18-100K
R19-2.2K
R20-100K

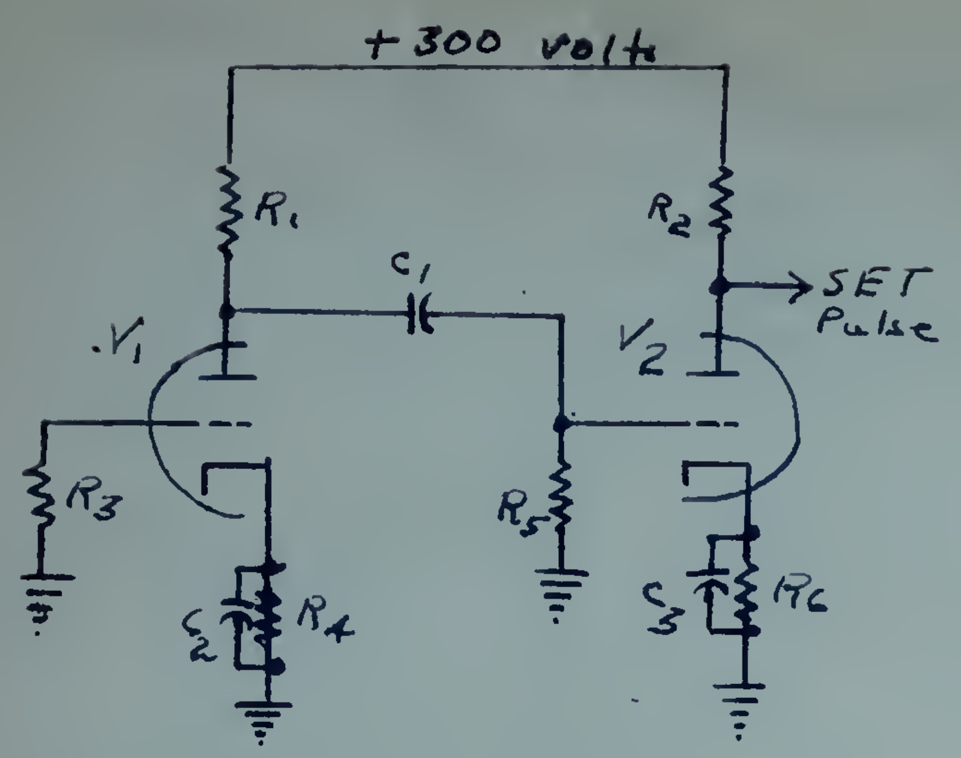
C1 -10μμf
C2 -50μμf
C3 -50μμf
C4 -.04μf
C5 -100μμf
C6 -50μμf

V1 -½6J6
V2 -½6J6

V3 -6J6
V4 -6AS6
V5 -½6SN7
V6 -Neon bulb

PLATE IV

Flip*Flop and Gate Circuit

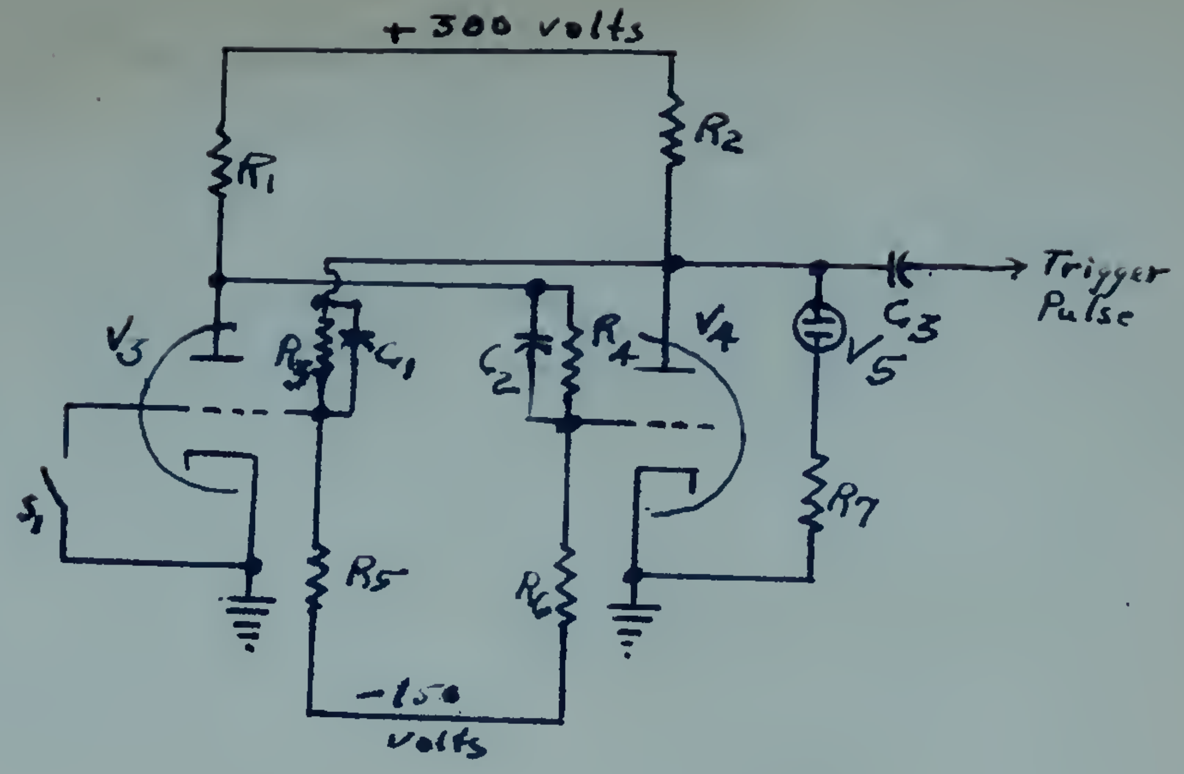


R1 -.1M
R2 -.1M
R3 -.1M
R4 -2.2K
R5 -.1M
R6 -2.2K

C1 -100μμf
C2 -2μf
C3 -2μf

V1 -½6SN7
V2 -½6SN7

SET Pulse Amplifier



R1 -68K
R2 -68K
R3 -82K
R4 -82K
R5 -250K
R6 -250K
R7 -220K
S1 -STSP switch

C1 -350μμf
C2 -350μμf
C3 -100μμf
V3 -½6SN7
V4 -½6SN7
V5 -Neon bubb

Pulse Source for One Shot Operation

PLATE V

Miscellaneous Circuits

Dial Reading	Counter Reading														
	Run Number														Probable
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Number
000	7	7	7	8	7	8	6	8	7	7	7	8	7	7	7
025	16	16	15	16	16										16
050	26	26	26	26	26										26
075	36	36	37	36	36										36
100	46	47	47	46	47	47	46	47	47	46	47	47	47	47	47
125	57	56	56	57	56										56
150	66	67	67	66	66										66
175	76	77	77	76	75										76
200	87	87	87	87	86	87	87	87	87	86	87	87	87	87	87
225	97	97	96	97	97										97
250	107	107	106	106	107										107
275	117	117	117	117	117										117
300	127	128	127	127	128	127	127	127	127	127	127	127	127	127	127
325	137	137	137	137	137										137
350	147	147	147	147	147										147
375	157	156	156	157	157										157
400	167	166	166	166	167	167	166	166	166	166	166	166	167	166	166
425	178	177	178	177	177										177
450	187	186	187	186	187	187									187
475	197	197	196	196	197										197
500	207	206	206	206	207	206	207	206	206	206	206	207	207	207	206
525	218	218	218	218	218										218
550	226	226	227	227	225										226
575	237	237	237	236	237										237
600	247	247	247	247	247	247	247	247	247	246	247	247	247	247	247
625	257	257	257	257	258										257
650	266	267	266	266	267										267
675	277	277	277	277	277										277
700	287	287	286	287	286	287	287	287	286	287	287	287	287	287	287
725	296	296	297	296	296										296
750	307	307	308	306	308										308
775	317	317	316	316	317										317
800	328	328	328	329	328	329	328	329	328	328	328	328	328	328	328
825	337	336	338	336	337										337
850	348	347	348	346	348										348
875	358	359	356	359	358										358
900	368	368	368	369	369	368	368	369	369	368	368	369	368	368	368

PLATE VI

Test data from converter operating on one shot basis.

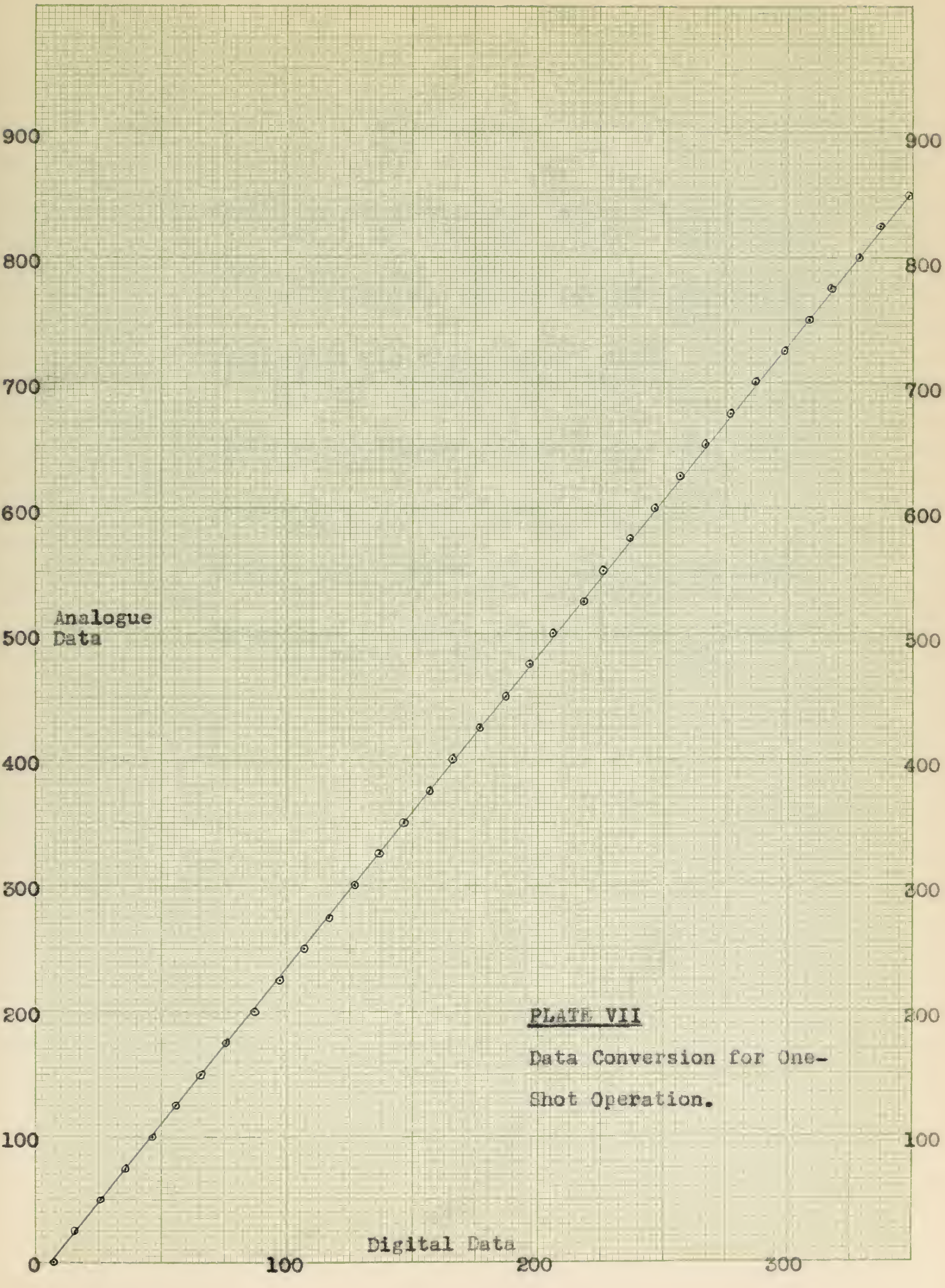


PLATE VII

Data Conversion for One-Shot Operation.

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